Remarks

I. Status of claims

Claims 1-20 were pending.

Dependent claims 21-26 have been added.

II. Claim rejections under 35 U.S.C. § 112

The Examiner has rejected claim under 35 U.S.C § 112, second paragraph, because "claim 20 states 'storing the communications module before…,' it should be storing the data channel."

The language of claim 20, however, is not indefinite. In particular, claim 20 depends from claim 18, which recites "A method of making a communications module." Therefore, there is no ambiguity about "the communications module" that is referred to in claim 20. The Examiner's attention is drawn to block 98 of the method shown in FIG. 5 and to page 7, line 8, through page 8, line 2, of the specification for a description of an exemplary embodiment of the subject matter of claim 20.

III. Claim rejections under 35 U.S.C. § 102

The Examiner has rejected claims 1, 2, 5, 8, 9, 13, and 18-20 under 35 U.S.C. § 102(e) over Bosnyak (U.S. 6,515,501).

A. Independent claim 1

Independent claim 1 recites:

> 1. A communications module, comprising:
>
> a data channel operable to translate data signals in at least one direction between a transmission cable interface and a host device interface and having a variably configurable termination impedance at a host device node connectable to a host device; and
>
> a termination impedance controller operable to set the variably configurable termination impedance of the data channel.

Bosnyak discloses a signal buffer that is mounted on a printed circuit board to maintain the signal integrity between integrated circuits (ICs) mounted on the same printed circuit board by matching impedances on the signal line traces on the printed circuit board interconnecting the ICs. In FIG. 7, Bosnyak shows that each of the signal buffers is implemented by an amplifier (referred to as a "gain circuit") having an input connected to an input signal trace and an output connected to an ouput signal trace, an input impedance circuit that shunts the amplifier input, and an output impedance circuit that shunts the amplifier output. In FIGS. 8A, 9A, and 10, Bosnyak shows that each of the impedance circuits is implemented passive circuit elements that are selectively connected between a signal line trace and a reference voltage (see col. 5, line 63 - col. 6, line 7).

In the rejection of claim 1, the Examiner has stated that Bosnyak discloses in FIG. 3 (emphasis added):

> a data channel (data path 108 stored within signal buffer (SB) 304 for retransmission) operable to translate data signals (reconstitute a signal; col. 7, lines 25-30) in at least one direction between a transmission line interface (signal buffer 302) (col. 4, lines 4-6) and a host device interface (interface between SB 304 and IC 104) (col. 7, lines 18-39; col. 6, lines 59-col. 7, line 4), and having a variably configurable termination impedance at a host device node (node at connection line between 304 and 104) connectable to a host device (104) (col. 3, line 66 - col. 4, line 4) (col. 4, lines 52-60)...

Thus, the Examiner has taken the position that the signal buffer 302 corresponds to a "transmission line interface", the "interface between SB 304 and IC 104" (which is simply the signal line trace 108 between the amplifier of the signal buffer and the input terminal of the IC 104) corresponds to a host device interface, and a that a "node at connection line between 304 and 104" corresponds to a host device node.

In this rejection, however, the Examiner has misread the language of claim 1. In particular, claim 1 does not recite a "transmission line interface." Instead, claim 1 recites "a data channel operable to translate data signals in at least one direction between a transmission cable interface and a host device interface" (emphasis added). The signal buffer 302 does not connect to a transmission cable and therefore is not a transmission cable interface nor does it include a transmission cable interface. Indeed, Bosnyak clearly teaches that the signal buffers 302 and 304 are implemented by amplifier circuits 506 and impedance circuits 508,

510 (see FIG. 5) that are configured as single in-line packages that are mounted on a printed circuit board 300 and are interconnected by signal line traces 108 on the printed circuit board 300 (see col. 4, lines 43-45). There is no reasonable basis for one skilled in the art at the time the invention was made to have believed that the signal line traces 108 on the printed circuit board 300 constituted a transmission cable. Accordingly, there is no reasonable basis for such a person to have believed that there was any transmission cable interface between the signal buffer 302 and the signal buffer 304, much less any need for any such transmission cable interface.

For at least these reasons, the Examiner's rejection of independent claim 1 under 35 U.S.C. § 102(e) over Bosnyak should be withdrawn.

B. Dependent claims 2, 5, 8, 9, and 13

Each of claims 2, 5, 8, 9, and 13 incorporates the features of independent claim 1 and therefore is patentable over Bosnyak for at least the same reasons explained above.

C. Independent claim 18

Independent claim 18 recites:

> 18. A method of making a communications module, comprising:
>
> obtaining a data channel operable to translate data signals in at least one direction between a transmission cable interface and a host device interface and having a variably configurable termination impedance at a host device node connectable to a host device;
>
> mounting the data channel in a housing having a first end connectable to a transmission cable and a second end connectable to a host device; and
>
> setting the variably configurable termination impedance of the data channel to a termination impedance value substantially matching a target host device termination impedance value.

Bosnyak does not teach that the signal buffer 304 is mounted in "a housing having a first end connectable to a transmission cable," as recited in claim 18. As explained above, Bosnyak clearly teaches that the signal buffer 304 is implemented by an amplifier circuit 506 and impedance circuits 508, 510 (see FIG. 5) that are configured as a single in-line package

that is mounted on a printed circuit board 300 and is connectable to signal line traces 108 on the printed circuit board 300 (see col. 4, lines 43-45).

For at least these reasons, the Examiner's rejection of independent claim 18 under 35 U.S.C. § 102(e) over Bosnyak should be withdrawn.

D. Dependent claims 19 and 20

Each of claims 19 and 20 incorporates the features of independent claim 18 and therefore is patentable over Bosnyak for at least the same reasons explained above.

IV. Claim rejections under 35 U.S.C. § 103

A. Claim 3

The Examiner has rejected claim 3 under 35 U.S.C. § 103(a) over Bosnyak in view of Jean (U.S. 6,407,639).

Claim 3 incorporates the features of independent claim 1. Jean does not make-up for the failure of Bosnyak to teach "a data channel operable to translate data signals in at least one direction between a transmission cable interface and a host device interface," as recited in claim 1. Indeed, the Examiner has cited Jean merely for the disclosure of "a variable resistance circuit [that] comprises a transistor (T) with a voltage-controlled resistance value..."

Therefore, claim 3 is patentable over Bosnyak and Jean for at least the same reasons explained above in connection with claim 1.

B. Claim 4

The Examiner has rejected claim 4 under 35 U.S.C. § 103(a) over Bosnyak in view of Bogli (U.S. 6,385,547).

Claim 4 incorporates the features of independent claim 1. Bogli does not make-up for the failure of Bosnyak to teach "a data channel operable to translate data signals in at least one direction between a transmission cable interface and a host device interface," as recited in claim 1. Indeed, the Examiner has cited Bogli merely for the disclosure of "a variable resistance circuit (28) [that] comprises a resistor (43) connected in series with a switch (37)..."

Therefore, claim 4 is patentable over Bosnyak and Bogli for at least the same reasons explained above in connection with claim 1.

C. Claim 6

The Examiner has rejected claim 6 under 35 U.S.C. § 103(a) over Bosnyak in view of Migayawa (U.S. 5,553,250) and unspecified and unsubstantiated prior art.

Claim 6 incorporates the features of independent claim 1. Neither Migayawa nor the unspecified and unsubstantiated prior art makes-up for the failure of Bosnyak to teach "a data channel operable to translate data signals in at least one direction between a transmission cable interface and a host device interface," as recited in claim 1.

Therefore, claim 6 is patentable over Bosnyak and Bogli for at least the same reasons explained above in connection with claim 1.

D. Claim 7

The Examiner has rejected claim 7 under 35 U.S.C. § 103(a) over Bosnyak in view of unspecified and unsubstantiated prior art.

Claim 7 incorporates the features of independent claim 1 and therefore is patentable over Bosnyak for at least the same reasons explained above in connection with claim 1.

E. Claims 10-12 and 14

The Examiner has rejected claims 10-12 and 14 under 35 U.S.C. § 103(a) over Bosnyak in view of Flickinger (U.S. 6,418,121).

Each of claims 10-12 and 14 incorporates the features of independent claim 1. Flickinger does not make-up for the failure of Bosnyak to teach "a data channel operable to translate data signals in at least one direction between a transmission cable interface and a host device interface," as recited in claim 1. Indeed, the Examiner has cited Flickinger for disclosing "a module implemented in accordance with a Giga-Bit Interface Converter (GBIC) configuration…"

Therefore, each of claims 10-12 and 14 is patentable over Bosnyak and Flickinger for at least the same reasons explained above in connection with claim 1. Claim 10 also is patentable over Bosnyak and Flickinger for the following additional reasons.

Claim 10 recites that "the host device interface end of the housing is pluggable into a receptacle of a host device." In the rejection of claim 10, the Examiner has stated that "It would have been obvious to one of ordinary skill in the art at the time the invention was made to plug the interface end of the housing into a receptacle of a host device in order to supply power to the module from the host." The rejection of claim 10, however, is premised on the Examiner's assertion that the signal buffer 304 corresponds to the communication module recited in claim 10 and that the IC 104 corresponds to the host device (see page 3, § 4 of the Office action). As explained above, in accordance with Bosnyak's teachings, signal buffer 304 is configured as a single in-line package that is mounted on a printed circuit board 300 and is connected to IC 104 on the printed circuit board by signal line traces 108 on the printed circuit board 300 (see col. 4, lines 43-45). There is no reasonable basis for one skilled in the art at the time the invention was made to have believed that the package of the IC 104 could be modified to include a receptacle in which the housing of the signal buffer 304 could be plugged.

For at least this additional reason, the Examiner's rejection of claim 10 under 35 U.S.C. § 103(a) over Bosnyak in view Flickinger of should be withdrawn.

F. Claims 15-17

The Examiner has rejected claims 15-17 under 35 U.S.C. § 103(a) over Bosnyak in view of Flickinger and Drost (U.S. 6,738,415).

Independent claim 15 recites:

> 15. A communications module, comprising:
>
> a receiver data channel operable to translate data signals from a transmission cable interface to a host device interface and a transmitter data channel operable to translate data signals from the host device interface to the transmission cable interface, wherein each of the receiver data channel and the transmitter data channel has a respective variably configurable termination impedance at a respective host device node connectable to the host device;
>
> a termination impedance controller operable to set the respective variably configurable termination impedance of each of the receiver data channel and the transmitter data channel; and
>
> a housing containing the receiver data channel, the transmitter data channel, and the termination impedance

controller, and having a transmission cable interface end connectable to a transmission cable and a host device interface end connectable to a host device.

Contrary to the Examiner's assertion, Bosnyak does not teach "a receiver data channel operable to translate data signals from a transmission cable interface to a host device interface and a transmitter data channel operable to translate data signals from the host device interface to the transmission cable interface," as recited in claim 15, for the same reasons explained above in connection with claim 1.

Each of claims 16 and 17 incorporates the features of independent claim 15. Neither Flickinger's disclosure of "a module implemented in accordance with a Giga-Bit Interface Converter (GBIC) configuration…" nor Drost's disclosure of "each of transmitter data channel (bidirectional data channel has a respective variably configurable termination impedance at a respective host device node …" makes-up for the failure of Bosnyak to teach the features of claim 15 discussed above.

V. Conclusion

For the reasons explained above, all of the pending claims are now in condition for allowance and should be allowed.

Charge any excess fees or apply any credits to Deposit Account No. 50-3718.

Respectfully submitted,

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